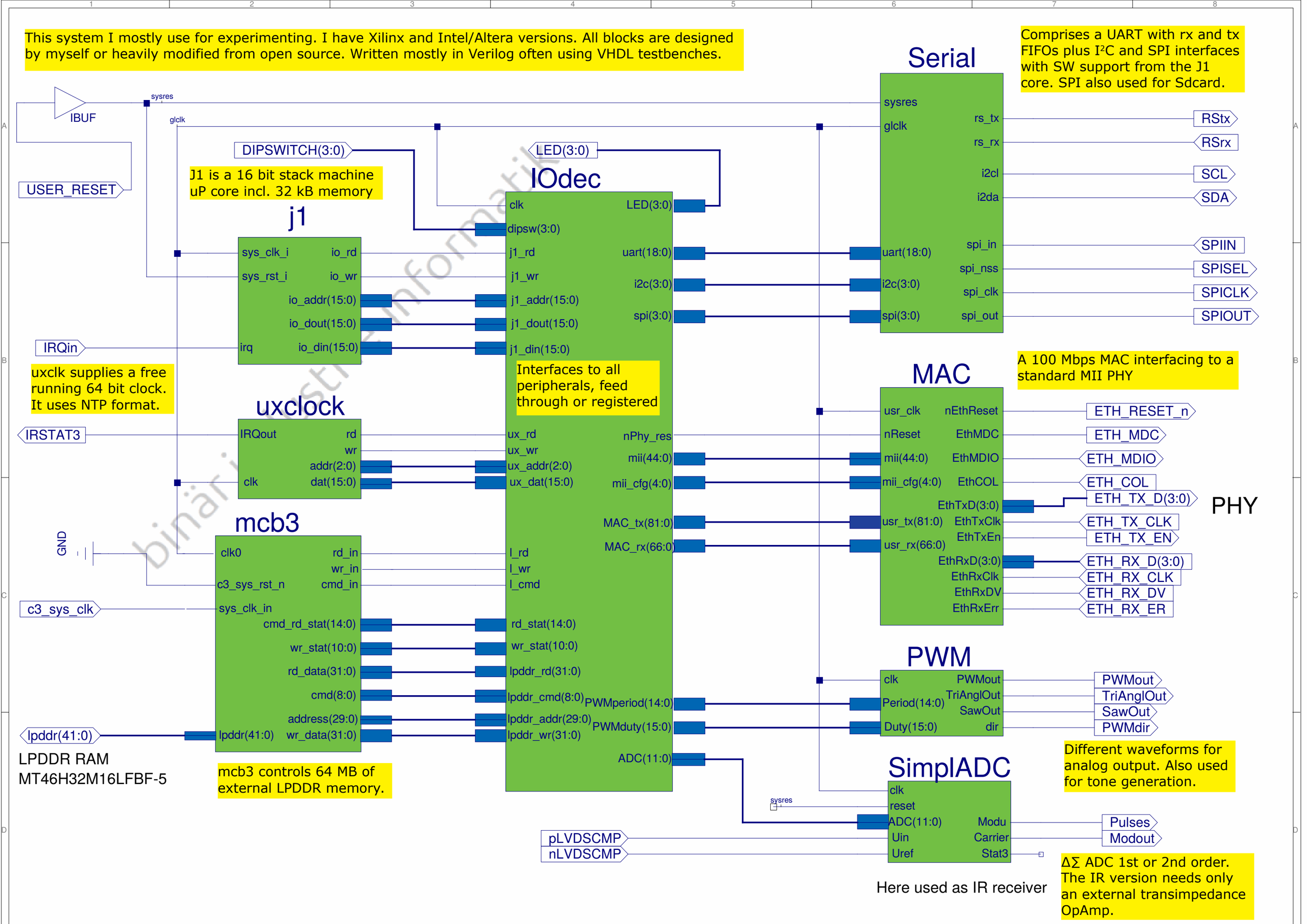This system I mostly use for experimenting. I have Xilinx and Intel/Altera versions. All blocks are designed by myself or heavily modified from open source. Written mostly in Verilog often using VHDL testbenches.